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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,015	DIAMOND ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The disclosure is objected to because of the following informalities: The copending application listed on page 4 of the specification be identified by serial number. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al.

a. Regarding claim 1, Wilen et al. **discloses** an output device (display monitor 135, Fig. 1) interfaced to a motherboard (computer system 100, Fig. 1); a fixed rendering device (on-board accelerated graphics port (AGP) device 150, Fig. 1) mounted to the motherboard (computer system 100) for generating information to be output on said output device (display monitor 135); a connector (AGP connector 152, Fig. 1) for attaching a field-changeable rendering card (external AGP device 154, Fig. 1) to the motherboard (computer system 100). Wilen et al. **does not explicitly disclose** a detection circuitry for detecting that a field-changeable rendering card housing a discrete rendering device is coupled to said connector and causing information from said field-changeable rendering card housing a discrete rendering device to be output o said output device, however, it **does disclose** the external AGP device 154 as an add-on graphics device located externally to the motherboard and an ADD card 156 that interfaces to the AGP connector. Further, Wilen et al. **discloses** a strapping scheme that indicates the

presence of ADD card 156 at the AGP connector housing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to make use of the same strapping scheme to detect presence of ADD card 156 for AGP device 154 **because** it provides an upgrade path for graphics capability if the internal graphics controller is not sufficient adding more user flexibility.

b. Regarding claim 2, Wilen et al. **discloses** wherein said fixed rendering device (on-board AGP device 150) is an integrated graphics processor (...device 150 is a graphic device...and is located on the motherboard that contains the processor 110...col. 3, lines 25-35) and said discrete rendering device is a discrete graphics processing unit (...the external AGP device 154 is an add-on...graphics device located externally to the motherboard...col. 3, lines 34-40).

4. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. as applied to claim 1 above and further in view of U.S. 2004/0228365 A1 to Kobayashi.

a. Regarding claim 3, Wilen et al. **is silent about** PCI express signal usage between said graphics processing unit from said integrated graphics processor in order to generate a plurality of signals for display on said output device. Kobayashi **discloses** an add-in graphics card supplanting the onboard graphics engine (See Fig. 23) and use of PCI express port (...the PCI express port is augmented to become compliant with...which can directly drive a...a add-in graphics card can supplant the onboard graphics engine...Fig. 23...page 9; paragraph 95, 96). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen et al. with the feature "PCI Express technology for communications between on-board and external add-on graphics controllers" as taught by Kobayashi

because PCI Express is a high-bandwidth, low pin count that maintains software compatibility with existing PCI infrastructure (page 9, paragraph 95).

b. Regarding claim 4, Wilen et al. **discloses** wherein said graphics processing unit is adapted to generate low voltage differential signaling (LVDS), digital video interface (DVI), television (TV) and video graphics array (VGA) signals (...the description of invention is directed to the digital video output...the invention can be practiced for other graphic modes...the DVO mode may include a digital video interface (DVI)...or low voltage differential signaling (LVDS)...the television set 146 receives the video signal...col. 2, lines 1-67; col. 3, lines 1-40).

5. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. as applied to claim 1 above and further in view of U.S. 6,570,561 B1 to Boesch et al.

a. Regarding claims 5 and 7, Wilen et al. **does not disclose** wherein said field-changeable rendering card does not house a discrete rendering device and acts as a passive loop-through card. Boesch et al. **discloses** support for higher resolution displays with an existing system board design to drive normal VGA and SVGA displays; while the translation board disclosed by Boesch et al. supports enhanced resolution display (col. 2, lines 5-40). Boesch et al. invention thus gives the option of supporting both, normal and enhanced graphics capabilities. With said translation board not being installed is similar to the passive loop-through card as recited in the claim limitation with signals being driven directly from the on-board graphics controller (Specification page 6, paragraph 28:..loop-through card...enables a...user to implement LVDS features without the need to implement...LVDS-capable devices...). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Wilen et al. with the feature "translation board option: Installed/Not installed" as taught

by Boesch et al. **because** it provides flexibility for the user to enhance the display capabilities at a later stage thus resulting in savings.

b. Regarding claim 6, Wilen et al. **discloses** wherein the discrete rendering device is a transmission minimized differential signaling (TMDS) transmitter (...the...external TMDS/LVDS devices 140 and 142 are graphic devices...external TMDS/LVDS device 142 is an add-on card...col. 3, lines 10-25). Wilen et al. **is silent about** field-changeble rendering card is a passive loop-through card. Boesch et al. **discloses** support for higher resolution displays with an existing system board design to drive normal VGA and SVGA displays; while the translation board disclosed by Boesch et al. supports enhanced resolution display (col. 2, lines 5-40). Boesch et al. invention thus gives the option of supporting both, normal and enhanced graphics capabilities. With said translation board not being installed is similar to the passive loop-through card as recited in the claim limitation with signals being driven directly from the on-board graphics controller (Specification page 6, paragraph 28:..loop-through card...enables a...user to implement LVDS features without the need to implement...LVDS-capable devices...). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Wilen et al. with the feature "translation board option: Installed/Not installed" as taught by Boesch et al. **because** it provides flexibility for the user to enhance the display capabilities at a later stage thus resulting in savings.

c. Regarding claims 8 and 9, Wilen et al. **discloses** wherein said graphics processing unit is adapted to generate low voltage differential signaling (LVDS), digital video interface (DVI), television (TV) and video graphics array (VGA) signals (...the description of invention is directed to the digital video output...the invention can be practiced for other graphic modes...the DVO mode may include a digital video interface

(DVI)...or low voltage differential signaling (LVDS)...the television set 146 receives the video signal...col. 2, lines 1-67; col. 3, lines 1-40).

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. as applied to claim 1 above and further in view of U.S. 6,893,268 B1 to Harari et al.

a. Regarding claim 10, Wilen et al. **does not disclose** wherein said field-changeable rendering card is an audio chip. Harari et al. **discloses** a removable mother/daughter peripheral card capable of processing audio (...the optional functional component 42 includes a data decompression module for decompressing...audio data..col. 13, lines 1-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen with the feature "audio processing module on a mother/daughter peripheral card" as taught by Harari et al. **because** it provides the user flexibility to upgrade audio performance.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:30AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh
Examiner, Art Unit 2671

dks
October 3, 2005

ULKA J. CHAUHAN
PRIMARY EXAMINER